CLAIMS

What is claimed is:

1. A process for reducing cross-talk noise in a circuit, comprising:

identifying a victim net in an integrated circuit;

determining a change in ground capacitance for the victim net to identify a noise amplitude less than or equal to a maximum allowable noise height;

selecting from a library at least one cell having an input capacitance for the victim net closest to the change in ground capacitance; and

coupling the at least one cell with the victim net.

2. The process of claim 1, wherein the at least one cell couples with the victim net using incremental routing.

3. The process of claim 1, wherein a value for the noise amplitude is determined through a calculation comprising:

$(R_dC_c) / (R_d(C_g + C_c) + (Slew_{agg}/2))$,

wherein R_d comprises a holding resistance of a driver of the victim net, C_c comprises a coupling capacitance between the victim net and an aggressor net, C_g comprises a ground capacitance of the victim net, and $Slew_{agg}$ comprises a slew of the aggressor net.

4. The process of claim 1, wherein determining the change in ground capacitance further a calculation comprising:

$(-C_c * N_s) / (N_m * N_A)$,

wherein, C_c comprises a coupling capacitance, N_s comprises a noise slack, N_m comprises a noise margin, and N_A comprises the noise amplitude.

5. The process of claim 4, wherein the noise slack comprises a difference between noise margin and noise amplitude.

6. The process of claim 1, further comprising testing an integrated circuit in response to connecting the at least one cell with the victim net.

7. The process of claim 6, wherein testing the integrated circuit further comprises one from a group consisting of conducing a timing analysis, conducting a change in slew analysis, conducting a power consumption analysis, and conducting an electromigration analysis.

8. The process of claim 6, further comprising rejecting the coupling of the at least one cell with the victim net in response to a result of the testing providing a value corresponding to an adverse effect on the integrated circuit.

9. A system for reducing cross-talk noise in a circuit, comprising:

a noise analyzer configured to identify a victim net in an integrated circuit;

an analysis engine configured to determine a value for a change in ground capacitance for a victim net, the change in ground capacitance providing a

noise amplitude for the victim net less than or equal to a maximum allowed noise height; and

a library configured to provide at least one cell having an input capacitance for coupling with the victim net, a total input capacitance for the victim net having a value substantially close to the change in ground capacitance.

10. The system of claim 9, wherein the noise analyzer is further configured to determine the value of the change in ground capacitance through a calculation comprising:

$(-C_c * N_s) / (N_m * N_A)$,

wherein, $C_c$comprises a coupling capacitance, N_s comprises a noise slack, N_m comprises a noise margin, and N_A comprises the noise amplitude.

11. The process of claim 10, wherein the noise slack comprises a difference between noise margin and noise amplitude

12. The system of claim 9, wherein a value for the noise amplitude is determined through a calculation comprising:

$(R_d C_c) / (R_d(C_g + C_c) + (Slew_{agg}/2))$,

wherein R_d comprises a holding resistance of a driver of the victim net, C_c comprises a coupling capacitance between the victim net and an aggressor net, C_g comprises a ground capacitance of the victim net, and $Slew_{agg}$ comprises a slew of the aggressor net.

13. The system of claim 9, further comprising a connection module configured to couple the at least one cell to the victim net.

14. The system of claim 13, further comprising a test module configured to test an integrated circuit incorporating the victim net in response to the coupling of the at least one cell to the victim net.

15. The system of claim 14, wherein the test comprises at least one test of a group consisting of a timing test, a slew test, power consumption test, and an electromigration test.

16. The system of claim 14, wherein the test module is further configured to reject coupling of the cell to the victim net in response to a result of the test providing a value corresponding to an adverse effect on the integrated circuit.

17. A system for reducing cross-talk noise in a very large scale integration ("VLSI") circuit, the system comprising:

a means for performing a noise analysis on a plurality of nets in the VLSI circuit;

a means for identifying at least one victim net among the plurality of nets, the victim net having a noise amplitude greater than a maximum allowable noise height;

a means for selecting a victim net from the at least one victim net;

a means for determining a change in a ground capacitance for the victim net such that the noise amplitude of the victim net is less than the maximum allowable noise height;

a means for selecting from a cell library a cell providing an input capacitance value substantially close to the value of the change in the ground capacitance; and

a means for coupling the cell with the victim net.

18. The system of claim 17, further comprising a means for testing the VLSI circuit in response to coupling the cell with the victim net.

19. The system of claim 18, wherein the means for testing the VLSI circuit rejects coupling the cell with the victim net in response to a test value associated with an adverse affect on the VLSI circuit.

20. The system of claim 19, wherein the means for testing the VLSI circuit includes a process for conducting a circuit timing test and the test value associated with the adverse affect on the VLSI circuit comprises a value less than a predetermined timing value.

21. The system of claim 19, wherein the means for testing the VLSI circuit includes a process for conducting a power consumption test and the test value associated with the adverse affect on the VLSI circuit comprises a value less than a predetermined power consumption value.

22. The system of claim 17, wherein the cell comprises one from a group consisting of an inverter logic element and a capacitance cell.

23. A process for reducing cross-talk noise in a very large scale integration ("VLSI") circuit, the process comprising:

performing a noise analysis on a plurality of nets in the VLSI circuit;

identifying at least one victim net among the plurality of nets, the victim net having a noise amplitude greater than a maximum allowable noise height;

selecting a victim net from the at least one victim net;

determining a change in a ground capacitance for the victim net such that the noise amplitude of the victim net is less than the maximum allowable noise height;

selecting from a cell library a cell providing an input capacitance value substantially close to the value of the change in the ground capacitance; and

coupling the cell with the victim net.

24. The process of claim 23, further comprising testing the VLSI circuit in response to the coupling of the cell with the victim net.

25. The process of claim 24, wherein the step of testing the VLSI circuit further comprises rejecting the coupling of the cell with the victim net in response to a test value associated with an adverse affect on the VLSI circuit.

26. The process of claim 25, wherein the step of testing the VLSI circuit comprises performing a timing test and the test value associated with the adverse affect on the VLSI circuit comprises a value less than a predetermined timing value.

27. The process of claim 25, wherein the step of testing the VLSI circuit comprises performing a power consumption test and the test value associated with the adverse

affect on the VLSI circuit comprises a value less than a predetermined power consumption value.

28. The system of claim 23, wherein the cell comprises one from a group consisting of an inverter logic element and a capacitance cell.